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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/955,542	09/18/2001	Lee D. Whetsel	TI-31727	9799

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2133	2

DATE MAILED: 02/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/955,542	Applicant(s) WHETSEL ET AL.	
	Examiner James C Kerveros	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: In the specification on page 1, line 2, under CROSS REFERENCE TO RELATED APPLICATIONS, the Application Number "09/803,588" does not correspond to the proper subject title. It should be changed to ---09/803,599---.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by James (US 5768289), issued June 16, 1998.

Regarding Claims 1-3, James discloses a process of operating a plurality of scan paths, such as registers 7 and 15, shown in FIG. 2 and register 7, shown in detailed in FIG. 1, comprising:

Sequentially accessing through the output serial (TDO) and shifting (TDI) data through each one of the scan paths registers, simultaneously accessing and loading parallel data between register (7) output lines into logic circuitry (6) at a first time and

simultaneously accessing and loading parallel data from the logic circuitry (6) lines into all the plurality of scan paths register (7) at a second time, FIG. 1 and 4.

Regarding Claim 4, James discloses a scan path arrangement within an integrated circuit, (Prior Art, FIG. 1, IC 5) including boundary-scan cells interposed between the device I/O pins (4) and core logic circuitry (6) to be tested, comprising:

A scan input terminal (TDI) and a scan output terminal (TDO), having a scan path shift register "boundary-scan register" 7 connected to the logic circuitry core logic circuitry (6), where the scan path has an input and an output corresponding to a serial data input and serial data output for boundary-scan cell (11) and (12), respectively, FIG. 1.

A memory (storage elements 43 and 45) of boundary-scan cell (12), that can be used to support either an input connected to boundary-scan cell 11 or an output pin connected to boundary-scan cell 12, where the memory is isolated from the logic circuitry (6), such that the memory has an input (D) and an output (Q), as shown in detailed in FIG. 3.

A first connection is formed between the scan input terminal (TDI) and the memory input (D), a second connection is formed between the memory output (Q) and the scan path input at cell (11), and a third connection is formed between the scan path output at cell (12) and the scan output terminal (TDO).

Regarding Claim 5, James discloses memory (D) and scan path (7), which are connected to a common clocking source, (CLOCKDR), FIG. 3.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James C Kerveros
Examiner
Art Unit 2133

By: _____

Gregory J. Lamarre
for
Albert DeCady
Primary Examiner

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03/02/2004
Non-Final Rejection